

PHASE SHIFT AND POWER FACTOR DIGITAL METER

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Abstract: This paper presents some aspects of the digital measurement of the phase and the power factor. An experimental model of a phase shift and power factor meter is also described.

Keywords: Phase and Power Factor Measurement, Digital Phase-Meter

INTRODUCTION

In the field of digital measurements, the phase shift and the power factor are important features that are useful in the quality evaluations of various electrical circuits and power consumers. The phase measurement is a useful method to estimate the distortions introduced by a certain electric or electronic circuit. All devices are characterised by a specific delay or response time that have different significances depending on the frequency of the input signal. When periodic signals are applied to the input of the devices, between the input and the output signal a delay can be defined and called phase shift. This delay has frequency dependant weight in the period of the said signal: the higher the frequency, the higher the influence of the delay. Measuring the amount of the delay in the period of the signal is a way to evaluate the behaviour of the device in the dynamic state.

The digital instruments dedicated to the phase shift measurement (the phase-meters) evaluate the time lag between homologue points in the evolution of the two signals. A time lag “ t_l ” between two signals with the period “ T ” means a phase shift of $j = t_l / T$. Usually, the function of the phase measurement is integrated with other functions in the complex digital meters. Nevertheless, dedicated instruments are built on the principle mentioned above.

In the power systems, the phase shift between the voltage and the current signals on each phase may be an important feature when qualitative characterisations must be made on certain consumers. As the phase shift itself φ is not relevant in the power circuits analysis, a synthetic value related to it is used instead: the power factor, $\cos\varphi$. The dedicated instrument ($\cos\varphi$ -meter) displays the values of the power factor in non-dimensional units. The present paper presents a digital implementation of a phase & $\cos\varphi$ -meter that evaluates both the phase shift and the power factor in variable frequency environments.

THEORETICAL BACKGROUND

The simplest digital phase-meters are built for fixed frequency. An oscillator with a constant output frequency is used to generate pulses counted in the phase shift corresponding to the time lag “ t_l ” (Serban 1996).

The measured phase shift will be displayed as:

$$j = 360 t_l / T_{osc}.$$

Using a digital technique to evaluate the time intervals t_l and T one can get the value of the phase shift. The method asks only to count the pulses generated by a quartz-stabilised oscillator in the specified time lag. The higher the frequency of the oscillator, the better the precision of the phase-meter. The resolution of the measurement depends on the number of the pulses that are count in the minimum time lag. I.e. for a $0,1^\circ$ resolution at least one pulse must be counted. For an entire period, a total number of $360/0,1=3600$ pulses must be counted. If the period of the main signal is sufficiently long, the pulses may be counted with no problems, but when the signal’s frequency is high, the counter’s speed becomes prohibitive and high quality counters must be used.

Usually, the digital phase-meters are featured with a few tens of kilohertz bandwidth.

A better instrument could be realised (Nicolau 1979) if more “ t_l ” and “ T ” intervals are considered in order to count the pulses from the oscillator (figure 1). The clock pulses from the oscillator are validated by the input AND gates 1 and 2 only on the positive half-periods of the two signals. The XOR gate selects only the bursts corresponding to the time lags “ t_l ” when the two signals evolve in different parts of the time axe. N pulses in the total number of validated bursts will represent these time lags. For each period there are two “ t_l ” intervals.

In the first counter the pulses corresponding to a certain N number of periods are counted. In order to get the value of the phase shift in the usual format (hexadecimal degrees), N is chosen as a multiple of 360 ($N=360k$). This number prescales the first counter. As long as the first counter counts the N clock pulses, the output of the XOR gate is validated and through gate 3 multiple bursts of pulses corresponding to the phase shift are passed in the second counter. The displayed value of the phase shift will be: $j = n / k$, where n is the number of pulses counted during all the time-lags corresponding to the phase shifts along the measuring time, and k is the number of periods along the measurement is developed. The global precision does not depend anymore on the frequency of the oscillator and, moreover, the noise influence is reduced down to zero as the number of signal periods that compose the measuring time may be of hundreds. The bandwidth extends from 1Hz to 1MHz.

The described schematic works when one can specify the number N of pulses used to prescale the first counter, representing the number of signal periods that compose the measuring time. In order to measure the phase shift for signals with variable frequency, an additional module

must be included in the diagram in figure 1, to evaluate the unknown period T.

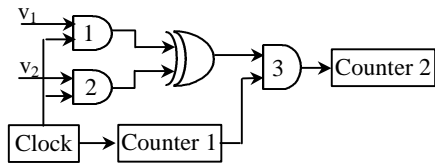


Figure 1. Digital Burst Phase-Meter

The instrument will include, in this case, a digital measurement controller to manage the operations and sequences of the measurement process.

PRACTICAL IMPLEMENTATION

A model for the phase and power factor meter was built with the main goal of evaluation of the phase shifts between two voltages (in order to obtain the phase characteristics for electric and electronic circuits), two currents or a voltage and a current (in order to evaluate the power factor in low voltage circuits).

The meter is structured in two modules: the analog input module and the digital module. Consequently, the function of the input module is to pick the input signals and shape them in a rectangular waveform with limited amplitude.

The input module contains four completely independent channels, two for current and two for voltage, with good individual insulation. The maximum voltage that strains the isolation between the input channels is the line voltage (380V). Each input channel's insulation is distributed in two sections: the power supply and the digital module input port (figure 2).

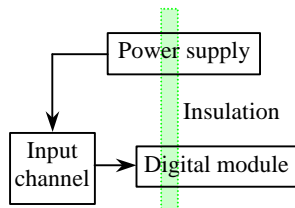


Figure 2. The Input Channels' Insulation

The power supply must have separate outputs for the four channels, each level of insulation being designed for the rated line voltage.

The signal transfer between any input channel and the digital module is made through an optocoupler with an adequate level of the insulation voltage and dynamic features.

The voltage and current input channels meet various conditions, but the most important is to introduce minimum supplemental phase errors. Noninductive resistive adapters were chosen in both situations: shunts - for current inputs and resistive dividers - for voltage inputs. The detailed schematics of the voltage and current input channels are shown in figure 3 and figure 4 respectively. Each input channel includes a simple protection circuitry, a high gain amplifier and a

comparator. The main rated features of the input channels are: $U_n = 380V$; $I_n = 10A$.

The minimum values for the input signals are 10mV for voltage and 10mA for current.

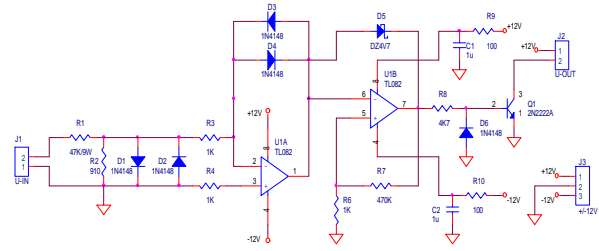


Figure 3. Voltage Input Channel

In order to avoid the saturation and/or the latch-up of the amplifier, a limited output voltage configuration was chosen, with opposite diodes in the negative feedback loop. For the very low input levels the amplifier acts as an open loop one, its very high gain producing a fast rise of the output signal and a well shaped rectangular output voltage. For normal and high input voltages, the limiting diodes avoid the saturation of the amplifier itself and of the next comparator. This way the comparator's switching performances are improved and few error sources are minimised.

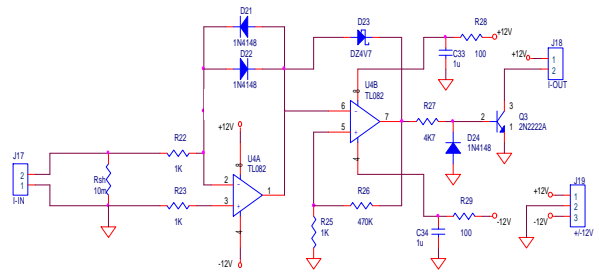


Figure 4. Current Input Channel

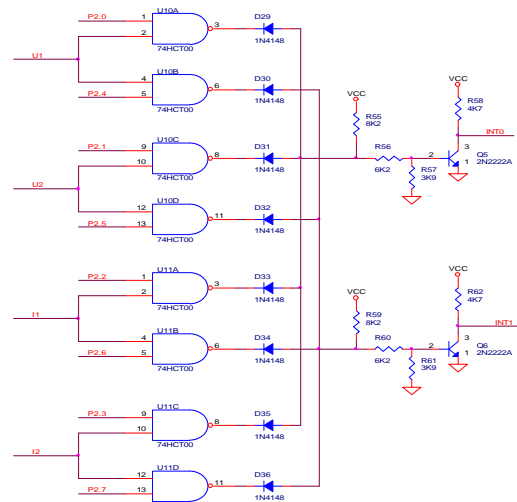


Figure 5. The Channel Selector

Measuring the phase shift, one must declare first the "time-fixed" signal considered as a reference and the

“time-floating” signal that is shifted with respect to the first. The input channel selector is a part of the digital module and allows selecting the reference and the secondary signals that define the phase shift.

The detailed schematic of the channel selector is shown in figure 5.

The digital module makes the selection of the prescribed input signals and evaluates the main period and the phase shift of the two signals. The power factor is also displayed. AT89S52 microcontroller (ATMEL 2001) was chosen to achieve all the operations, mainly because it allowed to drive also a digital display with no additional circuits and to select the inputs and the function of the meter (phase or power factor metering) using a main menu.

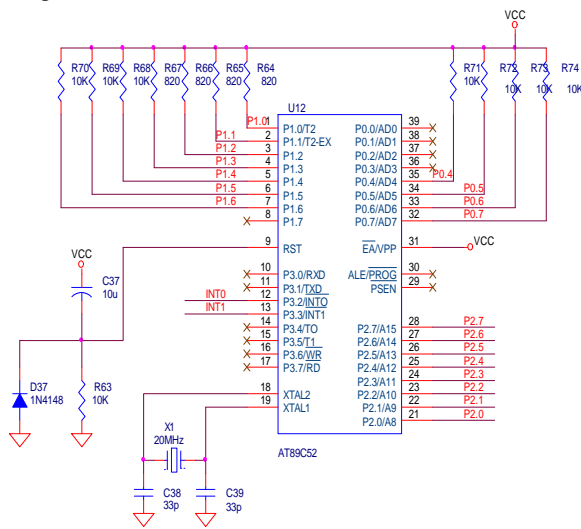


Figure 6. The Digital Module

All four ports of the microcontroller are used: P0 and P1 - for the human interface control (display and menu selection), P2 – for the channel selection and P3 – for the shaped signals inputs as interrupts.

The principle of the meter involves two operations: the main period “T” measurement and the relative time delay between the two signals “t_i” measurement. Next the phase shift is computed using the formula:

$$\varphi = 360 t_i / T \quad (1)$$

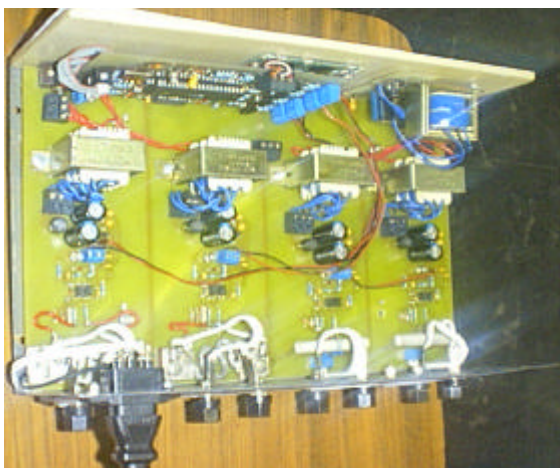


Figure 7. The Phase-Meter Experimental Model

The power factor is displayed after a table search depending on the value of the measured phase shift. The experimental model was realised using usual commercial devices. The analog and digital modules were built on different PCBs (figure 7).

The model of the digital module is shown in figure 8:

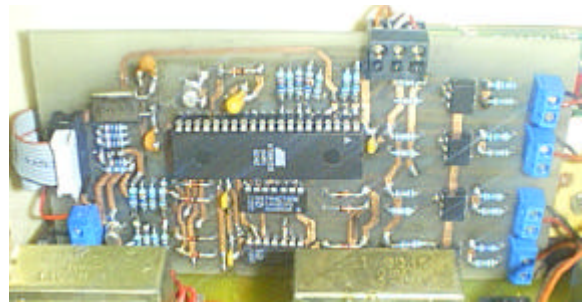


Figure 8. The Digital Module

SOFTWARE

The software was designed keeping in mind the main goals: the maximum precision of the phase shift and power factor measurement and the shortest algorithms. The time measurement uses 16 bit resolution and the arithmetic operations – 32 bit resolution, so all additional errors due to the inherent truncations are avoided.

The measurement is started on the falling edge of the rising front of the signals applied to the INTO and INT1 pins of the microcontroller. Both T2L and T2H registers of the T2 timer in AT89C52 are loaded with 0000h before any measurement, next INTO interrupt is enabled. When the first INTO comes, timer T2 receives the RUN command. T2 will be incremented every 0,6ms. When the second INTO interrupt comes, the T2 timer will be stopped. The two registers T2L and T2H are read and the result will compose the “T” operand that will be saved in temporary registers. After both registers’ content is saved, they receive a “reset” command and the timer T2 waits the next INTO interrupt. T2 is run again until INT1 interrupt becomes active and the timer it is stopped.

The content of the two registers are read and saved in the special function registers area as the “t_i” operand.

Appropriate routines are used to do the arithmetic calculus in hexagesimal base in order to determine the phase shift “φ”. The corresponding value of cosφ is searched in the memorised table. Both values are BCD and ASCII converted in order to be sent to the display’s controller. The measuring cycle replays on every 500ms.

ERROR ANALYSIS

Using the 16-bit timer T2 in the AT89C52 and a 20MHz main frequency, the absolute error for the time measuring is 0,6μs. The basic instrumental error is associated to and equals the phase-shift resolution (0,1°). For the power factor measurement, the absolute error is 0,004.

In addition to these main errors, supplemental under mentioned error components are to be considered:

- a) The small signals amplitudes, in conjunction with the fixed values of the hysteresis windows of the comparators;
- b) The jitter of the commutation moment of the comparator on each input channel, in conjunction with the signals' slew rate;
- c) The mis-synchronisation of the clock signal with the front of the validation signal;
- d) The small variations of the frequency of the signals that define the phase shift.

a) The moment of the comparator's switching is delayed from its ideal moment depending on the signal's relative amplitude. When the signal is small, then the moment of the switching comes later, because the fixed triggering level of the comparator is achieved later. The higher the signal's amplitude, the smaller the error component.

b) The moment that the comparator commutes (on any channel) strongly depends on the slew rate of the signal (figure 9). The slower the slew rate, the higher is the comparator's commutation delay. When the amplitude of the signal on the reference channel is much larger than the amplitude of the secondary signal, the measured value of the phase shift will be bigger than real. The error comes from the time lag \hat{a} , which delays the commutation of the comparator on the second channel with respect to the commutation of the comparator on the reference channel.

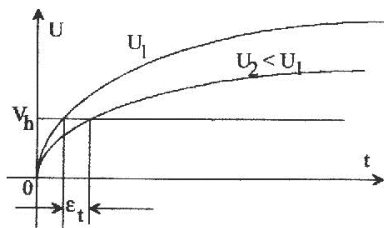


Figure 9. The influence of the signal's slew-rate

Mutually, when the reference signal's amplitude is smaller than the secondary signal's amplitude, the measured value of the phase-shift will be smaller than real.

c) The front of the signal that starts the incrementation of the phase-shift counter may be different from the clock front.

One clock tact may be lost because of that. The corresponding component of the global error will be equal to the quantum of one single clock period in the total time delay associated to the phase-shift. The bigger the phase-shift, the smaller the amount of one single clock pulse in the time period associated to the measured phase-shift.

d) The small variations in the frequency of the signals produced in the measurement time may produce an error component even if an actual signals' period measurement is achieved before any phase-shift measurement. When the signals' frequency has a small increase in the measurement time, the error component will be positive. At lower frequencies, the component of the error will be negative. This component must be taken into account with respect to the small variations in the main clock's frequency. A more realistic value can be predicted if average values are considered. In this case, this error component can easily be neglected.

The total dynamic error will be calculated by quadratic summation of the described components.

CONCLUSIONS

A digital phase and power factor meter was designed and built in order to obtain the phase characteristics of the electronic circuits and the analysis of the power transfer in electric circuits. The instrument may be associated to any power consumer. The use of a microcontroller for the functional control of the instrument allowed selecting any of the possible combinations of the input signals to measure the phase shift. The power factor has significance only for the proper combinations of the input channels. An error analysis reveals the main components of the global error of the digital meter. The instrument is useful in small signal circuit's analysis but also in the high power circuitry to evaluate the power transfer.

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